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Roll No. .....

BCA–303(N)

B. C. A. (Third Semester)
EXAMINATION, Dec., 2016

(New Course)

Paper Third

COMPUTER ARCHITECTURE AND ASSEMBLY LANGUAGE

Time : Three Hours] [*Maximum Marks : 75*

Note : Attempt questions from all Sections as directed.

Inst. : The candidates are required to answer only in serial order. If there are many parts of a question, answer them in continuation.

Section—A

(Short Answer Type Questions)

Note : All questions are compulsory. Each question carries 3 marks.

1. (A) Define Computer architecture in brief.

   (B) Discuss the functions of Program counter, Stack pointer and Flag register.

   (C) What is interrupt ? How are they handled by CPU ?

   (D) Why is I/O interface needed ? Give reasons.

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(E) What is microprocessor, microcomputer and microcontroller ? Describe in brief.

(F) Show the programming model of 8085 microprocessor. Describe zero, carry flags.

(G) Discuss the following instructions (8085) :

RAR

PUSH .B

LDAX B

along with an example showing its functionality.

(H) Write any *three* different addressing modes used in 8085 µP with one instruction from each category.

(I) Discuss about memory reference instruction–direct and indirect mode.

Section—B

(Long Answer Type Questions)

Note : Attempt any *two* questions. Each question carries 12 marks.

2. Discuss the steps involved in instruction cycle.

   Illustrate the steps involved in executing the given Program in 8085 Assembly language. The Program starts from location 2000 :

   MVI B, 76 H

   MVI A, F2H

   ADD B

   HLT

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3. (a) Show the block diagram of Control Unit of a basic computer with main memory 4096 × 16.

Assume instruction with one-bit mode and 3-bit opcode.

(b) Discuss interrupt cycle of basic computer.

4. (a) Discuss memory stack organization of CPU.

(b) How pipelining increases throughput of the computer system ? Show with an appropriate example.

5. (a) Show the organization of a BUS system for 8 registers with 4-bit each in a schematic diagram showing clearly the connections.

(b) Show the logic behind addition and subtraction with signed magnitude data show the hardware components needed to perform these operations.

Section—C

(Long Answer Type Questions)

Note : Attempt any *two* questions. Each question carries 12 marks.

6. (a) Discuss Priority Interrupt. Give a hardware based method to handle priority interrupt with a diagram.

(b) What is DMA ? Show the organization of DMA controller. Describe the steps involved in DMA process with example.

7. (a) Show only externally initiated signals and control/status signals of 8085 μP through a pin diagram.

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(b) Explain the function of ALE IO/$\overline{M}$, $\overline{RD}$, $\overline{WR}$ signal in 8085 μP.

Explain the need to demultiplex the bus AD_7-AD_0.

8. (a) Define Instruction cycle, Machine cycle, T-state of any 8085 instruction.

(b) Write valid instruction formats for the following :

(i) Conditional Jump instruction

(ii) Compare instruction

Also describe the functionalities of the above 8085 instructions.

9. (a) WAP in 8085 Assembly Language Program :

20 bytes of data are stored in memory location starting from 2040H to 2053H.

Transfer the entire block of data to new memory location starting at 2070H.

(b) (i) Show the memory interfacing of 2048 byte memory with 8085 μP in a schematic diagram. Show the address range.

(ii) Give register and memory content as each of the following instruction is being executed :

MVI B, 08

SUB A

LXI H, 2085

MOV M, B

INX H

MOV M, A

HLT

2900

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